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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,831	04/14/2004	Katsumi Fukumoto	577642000100	7735

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MORRISON & FOERSTER LLP
755 PAGE MILL RD
PALO ALTO, CA 94304-1018

EXAMINER	
WENDLER, ERIC J	
ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,831	FUKUMOTO, KATSUMI	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/8/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to the following communications: the Amendment after Non-Final Rejection filed on February 8, 2006.

2. Claims 1-8 are pending in the current application. Claims 1 and 5 are independent claims.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. JP 2003-109252, filed on April 14, 2003.

Response to Arguments

4. Applicant's arguments filed on February 8, 2006 have been fully considered but they are not persuasive. As per the rejection, Kikuchi teaches in Col. 5, lines 37-41, that "by reading the data from the protect memory cell whenever a command is executed, the device is inhibited from being written into or erased from if an erroneous command is taken in." The applicant correctly mentions that the examiner construes this teaching of Kikuchi as reading on claim 1, as it seems clear that the device of Kikuchi is inhibited from being written into or erasing from if an erroneous command is taken in because data is being read (first reading mode) from the protect memory cell whenever any command is executed (regardless of input control command). The applicant respectfully submits that Kikuchi fails to teach or suggest "setting the first reading mode, which is a mode of reading from the memory array where information such as programs and data are stored, regardless of the input control command, in a

data protection status where the programming and erasing modes are inhibited." The applicant also respectively submits that Kikuchi fails to teach or suggest "setting an inner level of a control command input circuit to an inner level corresponding to the first reading mode regardless of an input level of the control command, in a data protection status where the programming mode and the erase mode are inhibited" as recited in claim 5 since claim 5, like claim 1, recites that the first reading mode is "of reading out data from a memory array." However, as previously mentioned, Kikuchi indeed teaches a protect memory cell **116** that performs all these functions. Kikuchi specifically teaches, in Col. 6, lines 40-47, that this "protect memory cell **116** is composed of a single memory cell transistor provided in the memory cell array **106**." Therefore, the reading mode that is set regardless of the input control command is indeed a mode of reading from the memory array since the protect memory cell is provided in the memory cell array. The rejections listed below are therefore maintained.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA (Applicant Admitted Prior Art) in view of the US Patent to Kikuchi et al (5,381,369).

7. **Regarding claim 1,** the AAPA discloses an erroneous operation preventing circuit of an electrically rewritable non-volatile memory device for setting one or more operational modes of a plurality of operational modes including at least a first reading mode of reading out data from a memory array, a programming mode of writing data to the memory array, an erasing mode of erasing data from the memory array, and a second reading mode of reading out data not stored in the memory array, in accordance with an input control command, and performing a predetermined process in the set operational modes (paragraph 0006; Table 1). The AAPA does not teach an operational mode enforcing circuit for setting the first reading mode regardless of the input control command, in a data protection status where the programming mode and the erasing mode are inhibited from being set in accordance with a control signal for protecting predetermined data. Kikuchi teaches (column 4, lines 67-68, column 5, lines 1-2; and column 5, lines 26-27, 37-41) a circuit that sets a reading mode in a data protection status where the programming and erasing modes are inhibited from being set in accordance with a control signal for protecting predetermined data, regardless of an input control command, as the data is read from the protect circuit whenever any command is executed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the teaching of Kikuchi to the teaching of the AAPA. The AAPA, in essence, teaches data protection by write/erase inhibit only on certain input control commands. Combining the teaching of Kikuchi to the AAPA would give the obviously superior method of data protection by write/erase inhibit on every command.

8. **Regarding claim 5,** the AAPA teaches all that is discussed above but further fails to teach the operational mode enforcing circuit setting an inner level of a control command input circuit to an inner level corresponding to the first reading mode. Kikuchi teaches, in Fig. 10, the outputs of the write and erase control circuits and the output of the protect circuit going into two NOR gates, which can be considered an inner level of a control command input circuit, similar to OR gate (**7**) of the present application. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the teaching of Kikuchi to the teaching of the AAPA for the purpose of further ensuring that erroneous data would not be written to the memory array.

9. **Regarding claim 2 and 6,** the AAPA further teaches a protection status setting unit which sets a certain area of the memory array under data protection status (paragraph 0020 of the present application).

10. **Regarding claim 3 and 7,** the AAPA further teaches an operational mode where the programming and erasing modes are not inhibited or enabled in accordance with an input control command that determines the protection status (paragraph 0020 of the present application).

11. **Regarding claim 4 and 8,** the AAPA further teaches (paragraph 0006 of the present application) one or more command signals that correspond to each one of different operations, namely reading, writing, and erasing operations, and that these command signals originate from a writing/erasing circuit.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJW
4/20/06